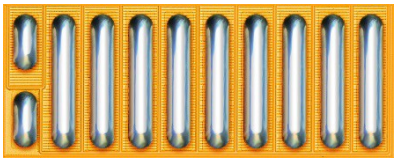
EPC2001C_55 – Enhancement-Mode Power Transistor
Preliminary Specification Sheet

Features:

- V_{DS}, 100 V
- Maximum $R_{DS(on)}$, 7 mΩ
- I_D, 36 A



EPC2001C_55 eGaN® FETs are supplied in passivated die form with solder bars.
Die Size: 4.1 mm x 1.6 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150˚C)	120	
I_D	Continuous (T_A = 25˚C, $R_{\theta JA}$ = 7.3 ˚C/W)	36	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	150	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	˚C
T_{STG}	Storage Temperature	-55 to 150	

Static Characteristics (T_J = 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	100			V
I_{DSS}	Drain Source Leakage	V_{DS} = 80 V, V_{GS} = 0 V, T_J = 25 °C		100	250	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = -55 °C		10	250	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V, T_J = 25 °C		1	5	mA
		V_{GS} = 5 V, T_J = -55 °C		0.1	5	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V, T_J = 25 °C		0.1	0.25	mA
		V_{GS} = -4 V, T_J = -55 °C		0.01	0.25	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 5 mA, T_J = 25 °C	0.8	1.4	2.5	V
		V_{DS} = V_{GS}, I_D = 5 mA, T_J = -55 °C	0.8	1.6	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 25 A, T_J = 25 °C		5.6	7	mΩ
		V_{GS} = 5 V, I_D = 25 A, T_J = -55 °C		3.7	5	mΩ

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	2	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	54	˚C/W

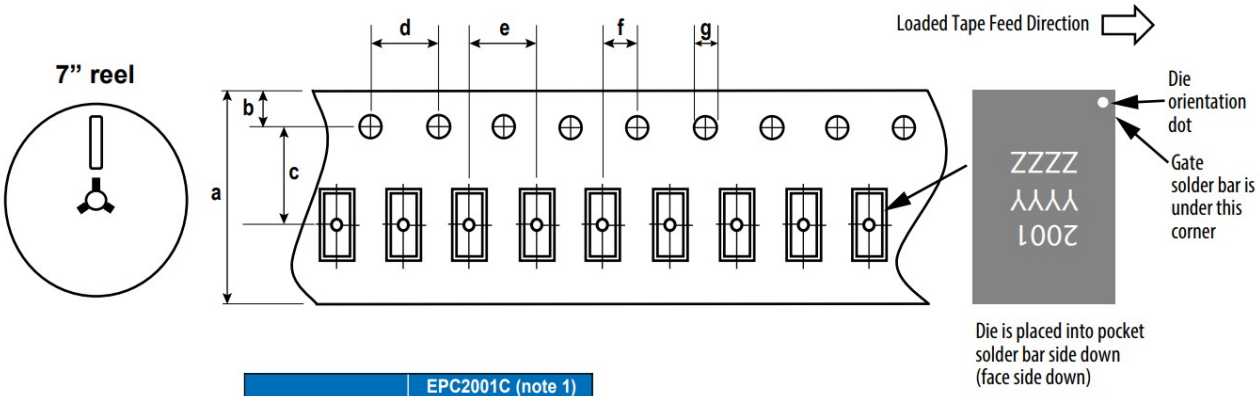
Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		770	90	pF
C_{RSS}	Reverse Transfer			10	15	
C_{OSS}	Output Capacitance			430	65	
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D=25 A		7.5	9	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 25 A		2.4		
Q_{GD}	Gate-to-Drain Charge			1.2	2	
$Q_{G(TH)}$	Gate Charge at Threshold			1.6		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		31	45	
Q_{RR}	Source-Drain Recovery			0		

All measurements were done with substrate shorted to source.

TAPE AND REEL CONFIGURATION

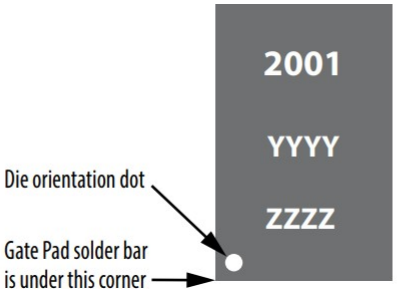
4mm pitch, 12mm wide tape on 7" reel



	EPC2001C (note 1)		
Dimension (mm)	target	min	max
a	12.0	11.7	12.3
b	1.75	1.65	1.85
c (note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

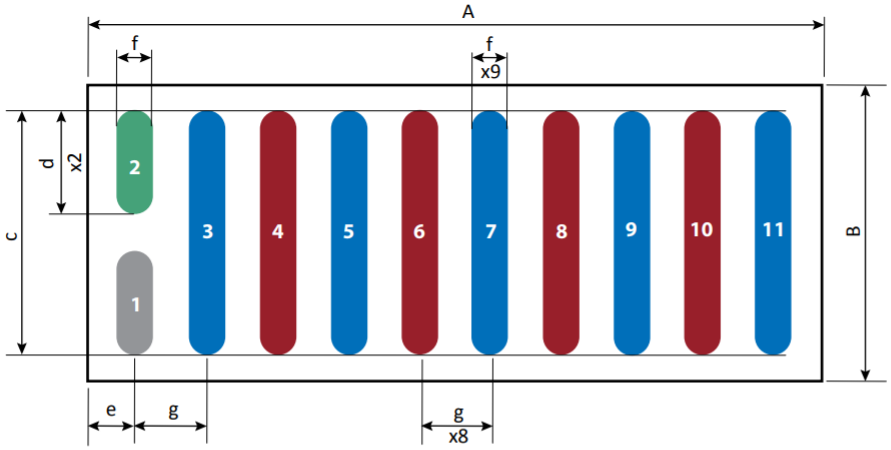
DIE MARKINGS



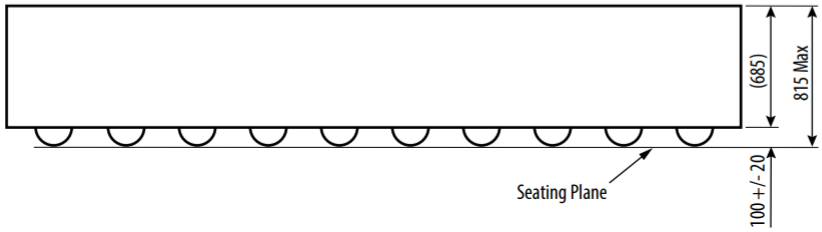
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2001C	2001	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



Side View

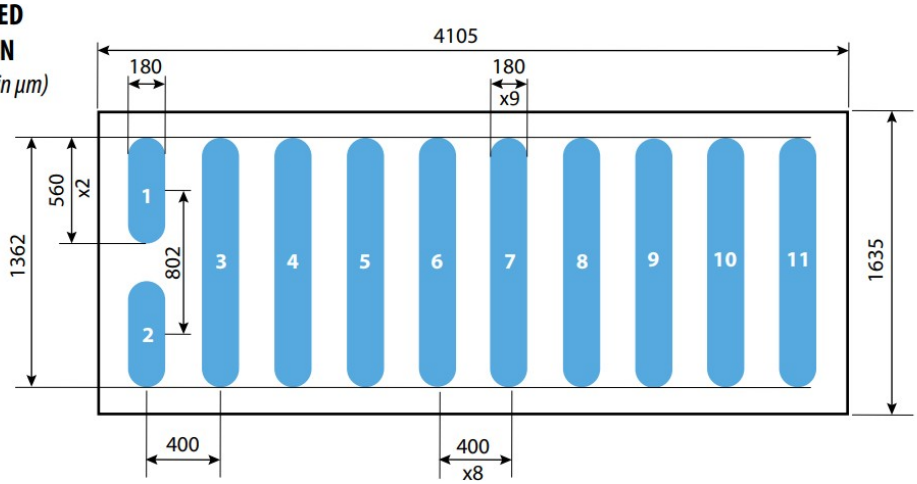


DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4075	4105	4135
B	1602	1635	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Pad no. 1 is Gate;
Pads no. 3, 5, 7, 9, 11 are Drain;
Pads no. 4, 6, 8, 10 are Source;
Pad no. 2 is Substrate.

RECOMMENDED LAND PATTERN

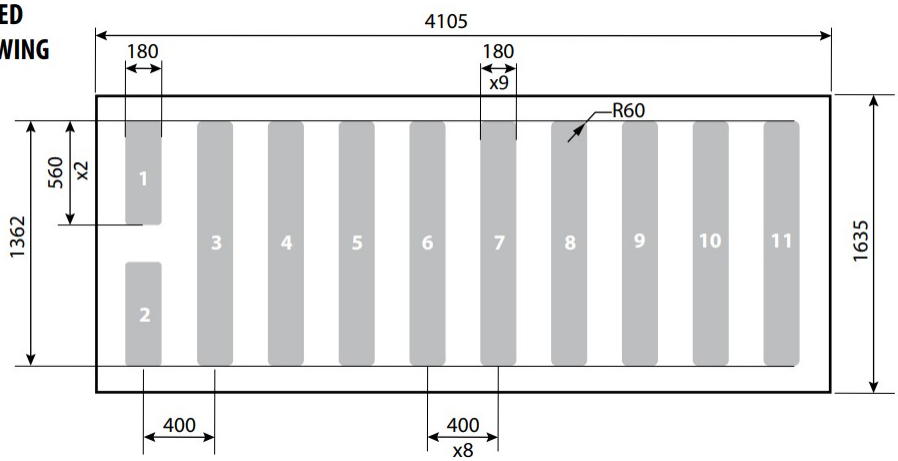
(measurements in µm)



The land pattern is solder mask defined.

Pad no. 1 is Gate;
Pads no. 3, 5, 7, 9, 11 are Drain;
Pads no. 4, 6, 8, 10 are Source;
Pad no. 2 is Substrate.

RECOMMENDED STENCIL DRAWING
(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Revised September 30, 2019