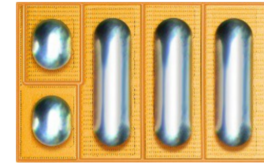
EPC2014C_55 – Enhancement-Mode Power Transistor
Preliminary Specification Sheet

Features:

- V_{DS}, 40 V
- Maximum $R_{DS(on)}$, 16 mΩ
- I_D, 10 A



EPC2014C_55 eGaN® FETs are supplied in passivated die form with solder bars.
Die Size: 1.7 mm x 1.1 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150˚C)	48	
I_D	Continuous (T_A = 25˚C, $R_{\theta JA}$ = 43 ˚C/W)	10	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	60	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	˚C
T_{STG}	Storage Temperature	-55 to 150	

Static Characteristics (T_J = 25˚C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	40			V
I_{DSS}	Drain Source Leakage	V_{DS} = 32 V, V_{GS} = 0 V, T_J = 25 °C		50	100	µA
		V_{DS} = 32 V, V_{GS} = 0 V, T_J = -55 °C		4	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V, T_J = 25 °C		0.4	2	mA
		V_{GS} = 5 V, T_J = -55 °C		0.04	2	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V, T_J = 25 °C		0.1	0.25	mA
		V_{GS} = -4 V, T_J = -55 °C		0.004	0.25	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 2 mA, T_J = 25 °C	0.8	1.4	2.5	V
		V_{DS} = V_{GS}, I_D = 2 mA, T_J = -55 °C	0.8	1.6	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 25 A, T_J = 25 °C		12	16	mΩ
		V_{GS} = 5 V, I_D = 25 A, T_J = -55 °C		8	11.5	mΩ

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.6	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	9.3	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	80	˚C/W

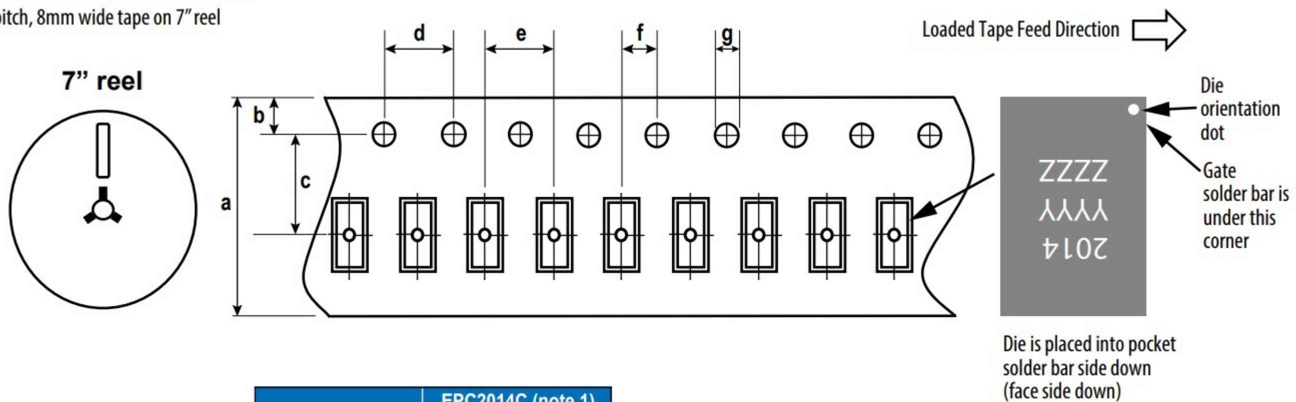
Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V		220	30	pF
C_{RSS}	Reverse Transfer			6.5	9.5	
C_{OSS}	Output Capacitance			150	21	
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 20 V, V_{GS} = 5 V, I_D = 10 A		2	2.5	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 20 V, I_D = 10 A		0.7		
Q_{GD}	Gate-to-Drain Charge			0.3	0.5	
$Q_{G(TH)}$	Gate Charge at Threshold			0.5		
Q_{OSS}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V		4	6	
Q_{RR}	Source-Drain Recovery			0		

All measurements were done with substrate shorted to source.

TAPE AND REEL CONFIGURATION

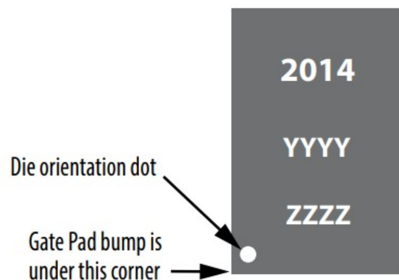
4mm pitch, 8mm wide tape on 7" reel



	EPC2014C (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

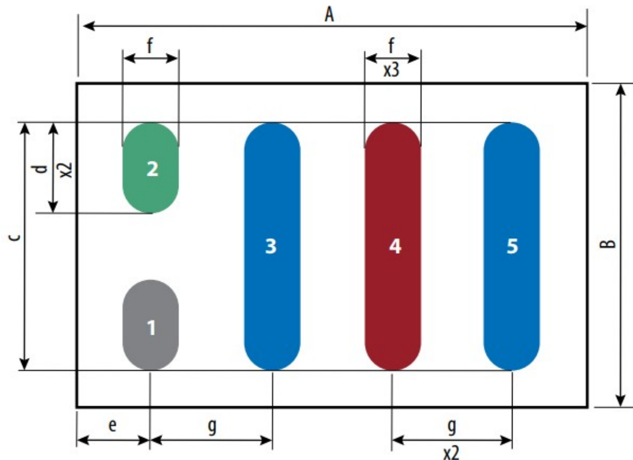
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS

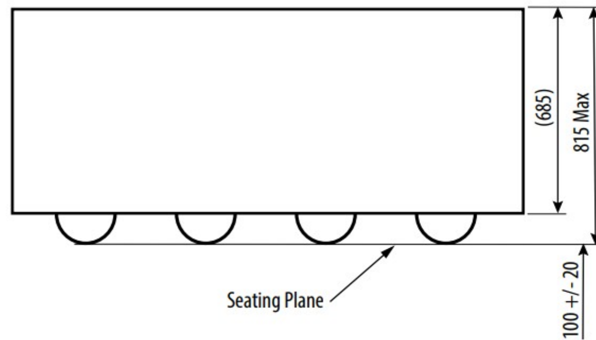


Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2014C	2014	YYYY	ZZZZ

DIE OUTLINE
Solder Bar View



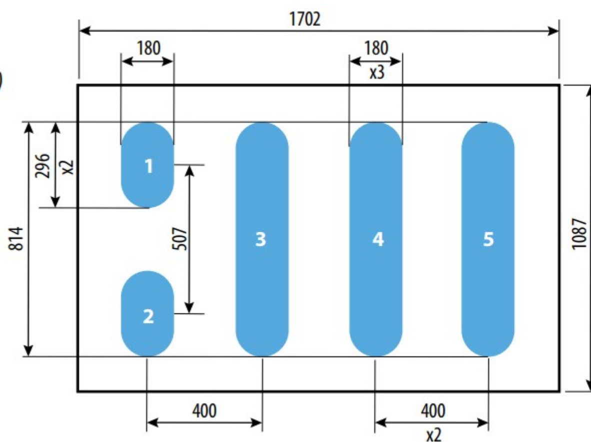
Side View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1672	1702	1732
B	1057	1087	1117
c	829	834	839
d	311	316	321
e	235	250	265
f	195	200	205
g	400	400	400

Pad no. 1 is Gate;
Pad no. 2 is Substrate;
Pads no. 3 and 5 are Drain;
Pad no. 4 is Source

RECOMMENDED LAND PATTERN
(measurements in µm)



The land pattern is solder mask defined
Solder mask is 10 µm smaller per side than bump

Pad no. 1 is Gate
Pad no. 2 is Substrate
Pads no. 3 and 5 are Drain
Pad no. 4 is Source

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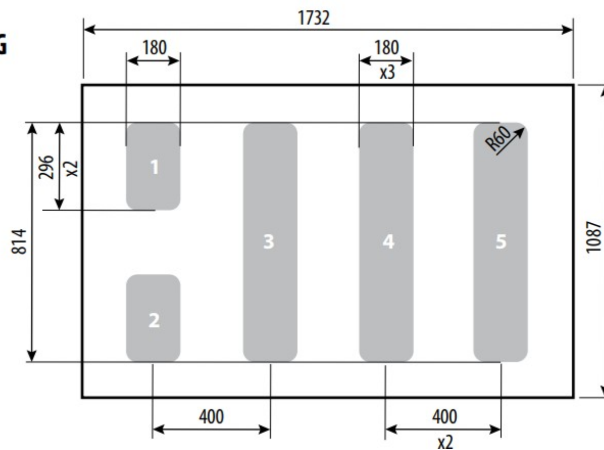
RECOMMENDED STENCIL DRAWING
(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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