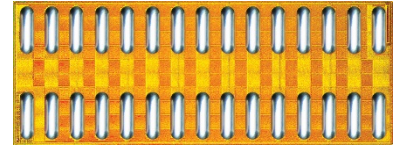


# EPC2022\_55 – Enhancement-Mode Power Transistor Preliminary Specification Sheet

## Features:

- $V_{DS}$ , 100 V
- Maximum  $R_{DS(on)}$ , 3.2 m $\Omega$
- $I_D$ , 90 A



EPC2022\_55 eGaN® FETs are supplied in passivated die form with solder bars.  
**Die Size: 6.05 mm x 2.3 mm**

Maximum Ratings			
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150°C)	120	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 2.5^\circ\text{C/W}$ )	90	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	290	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	

Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)							
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 900 \mu\text{A}$		100		V	
$I_{DSS}$	Drain Source Leakage	$V_{DS} = 80 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 25^\circ\text{C}$			100	700	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = -55^\circ\text{C}$			25	700	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$ , $T_J = 25^\circ\text{C}$			1	9	mA
		$V_{GS} = 5 \text{ V}$ , $T_J = -55^\circ\text{C}$			0.25	9	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$ , $T_J = 25^\circ\text{C}$			0.1	0.7	mA
		$V_{GS} = -4 \text{ V}$ , $T_J = -55^\circ\text{C}$			0.025	0.7	mA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 13 \text{ mA}$ , $T_J = 25^\circ\text{C}$		0.8	1.4	2.5	V
		$V_{DS} = V_{GS}$ , $I_D = 13 \text{ mA}$ , $T_J = -55^\circ\text{C}$		0.8	1.6	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 25 \text{ A}$ , $T_J = 25^\circ\text{C}$			2.4	3.2	m $\Omega$
		$V_{GS} = 5 \text{ V}$ , $I_D = 25 \text{ A}$ , $T_J = -55^\circ\text{C}$			1.6	2.3	m $\Omega$

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	42	°C/W

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.  
 See [http://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

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## Preliminary Specification Sheet

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ISS}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		1400	1680	pF
$C_{RSS}$	Reverse Transfer			7		
$C_{OSS}$	Output Capacitance			840	1260	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		1090		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1410		
$R_G$	Gate Resistance			0.3		$\Omega$
$Q_G$	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 25\text{ A}$		13	16	nC
$Q_{GS}$	Gate-to-Source Charge	$V_{DS} = 50\text{ V}, I_D = 25\text{ A}$		3.4		
$Q_{GD}$	Gate-to-Drain Charge			2.4		
$Q_{G(TH)}$	Gate Charge at Threshold			2.1		
$Q_{OSS}$	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		71	107	
$Q_{RR}$	Source-Drain Recovery			0		

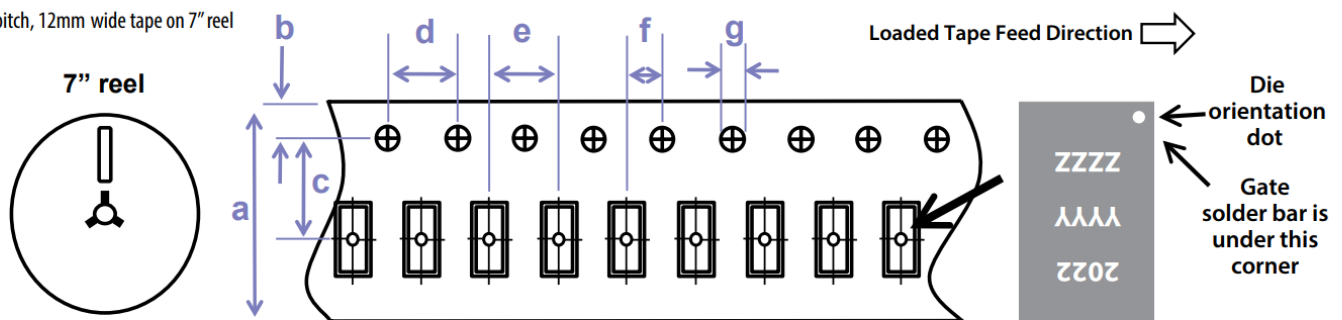
All measurements were done with substrate shorted to source.

Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$

### TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel



Die is placed into pocket  
solder bar side down  
(face side down)

Dimension (mm)	EPC2022 (note 1)		
	target	min	max
a	12.00	11.70	12.30
b	1.75	1.65	1.85
c (see note)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

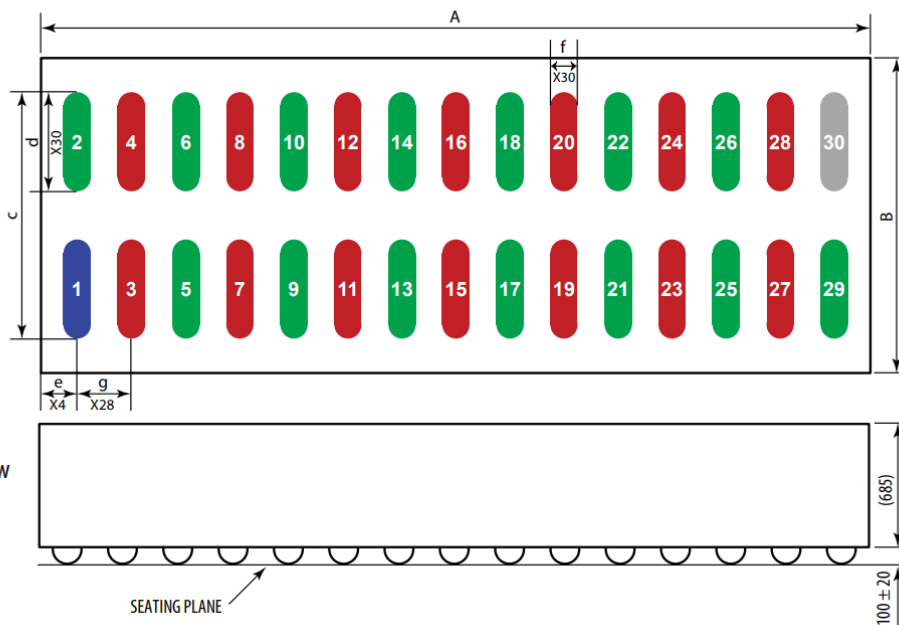
# EPC2022\_55 – Enhancement-Mode Power Transistor Preliminary Specification Sheet

## DIE MARKINGS

Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2022	2022	YYYY	ZZZZ

## DIE OUTLINE

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400

Pad 1 is Gate

Pads 2,5,6,9,10,13,14,17,18,21,22,

25,26,29 are Source

Pads 3,4,7,8,11,12,15,16,19,20,23,

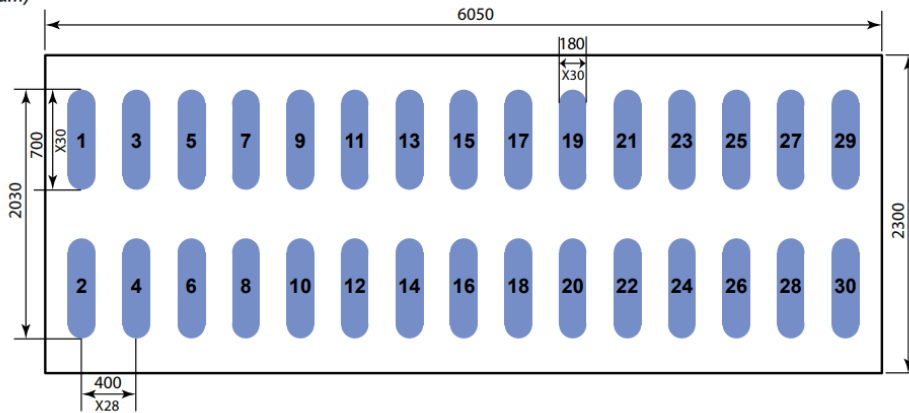
24,27,28 are Drain

Pad 30 is Substrate

# EPC2022\_55 – Enhancement-Mode Power Transistor Preliminary Specification Sheet

## RECOMMENDED LAND PATTERN

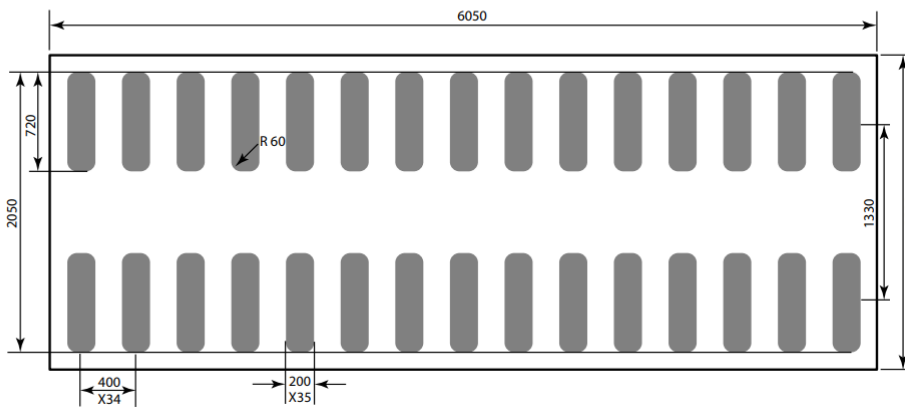
(units in  $\mu\text{m}$ )



Land pattern is solder mask defined  
Solder mask opening is 180  $\mu\text{m}$   
It is recommended to have on-Cu trace  
PCB vias

## RECOMMENDED STENCIL DRAWING

(units in  $\mu\text{m}$ )



Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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Revised January, 2019