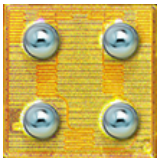
EPC2038_55 – Enhancement-Mode Power Transistor
Preliminary Specification Sheet

Features:

- V_{DS}, 100 V
- Internal Gate Diode
- Maximum $R_{DS(on)}$, 3300 mΩ
- I_D, 0.5 A



EPC2038_55 eGaN® FETs are supplied in passivated die form with solder bars.
Die Size: 0.9 mm x 0.9 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150˚C)	120	
I_D	Continuous (T_A = 25˚C, $R_{\theta JA}$ = 100 ˚C/W)	0.5	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	0.5	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	100			V
I_{DSS}	Drain Source Leakage	V_{DS} = 80 V, V_{GS} = 0 V, T_J = 25 °C		20	100	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = -55 °C		0.2	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V, T_J = 25 °C		0.1	500	µA
		V_{GS} = 5 V, T_J = -55 °C		0.01	500	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.1 mA, T_J = 25 °C	0.8	1.4	2.5	V
		V_{DS} = V_{GS}, I_D = 0.1 mA, T_J = -55 °C	0.8	1.6	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 0.05 A, T_J = 25 °C		2100	3300	mΩ
		V_{GS} = 5 V, I_D = 0.05 A, T_J = -55 °C		1400	2400	mΩ

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	27	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	91	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	100	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		7	8.4	pF
C_{RSS}	Reverse Transfer			0.02		
C_{OSS}	Output Capacitance			1.6	2.4	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		2.2		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			2.7		
R_G	Gate Resistance			4.8		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D= 0.05 A		44		nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D= 0.05 A		20		
Q_{GD}	Gate-to-Drain Charge			4		
$Q_{G(TH)}$	Gate Charge at Threshold			18		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		134		
Q_{RR}	Source-Drain Recovery			0		

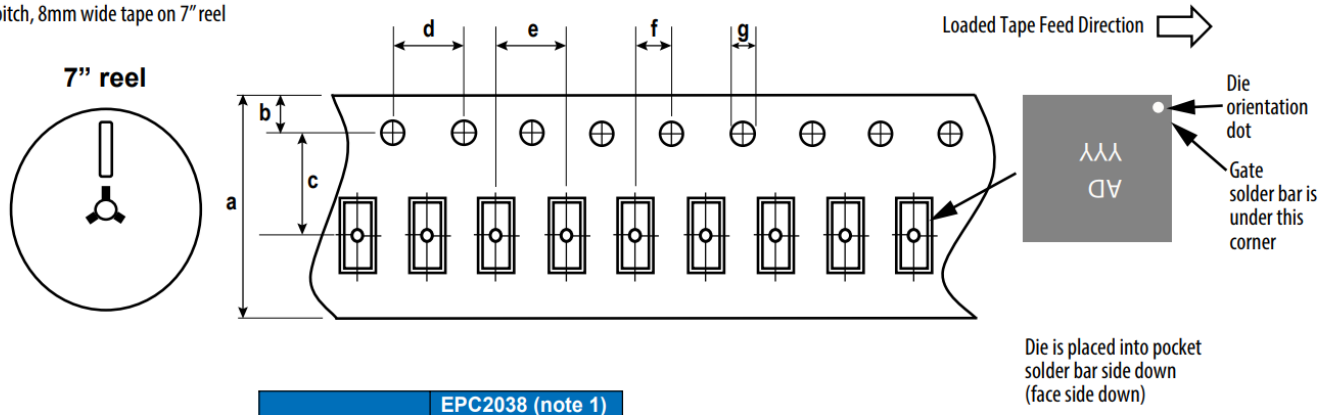
All measurements were done with substrate shorted to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 50% BV_{DSS}

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 50% BV_{DSS}

TAPE AND REEL CONFIGURATION

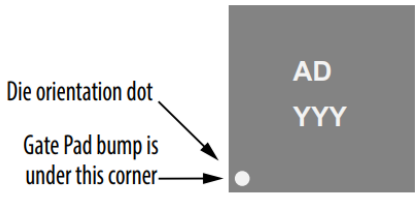
4mm pitch, 8mm wide tape on 7" reel



	EPC2038 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

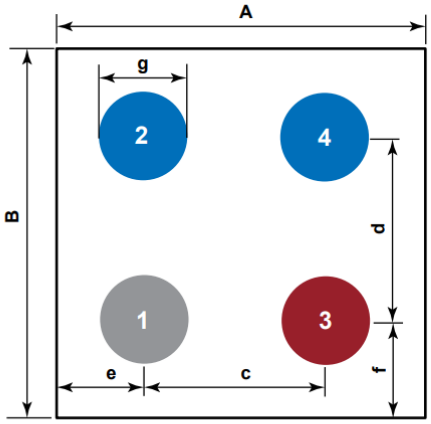
DIE MARKINGS



Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking line 2
EPC2038	AD	YYY

DIE OUTLINE

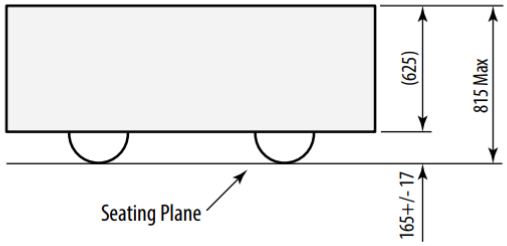
Solder Bump View



Pad 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

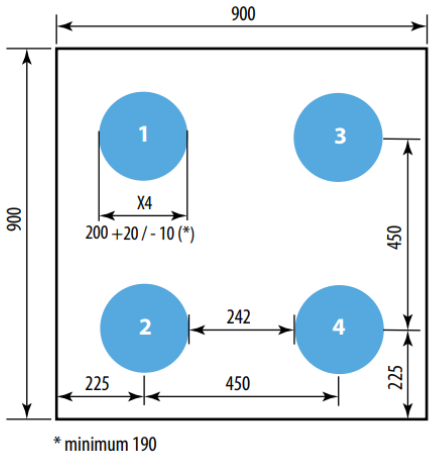
DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)



The land pattern is solder mask defined

Solder mask is 10 µm smaller per side than bump

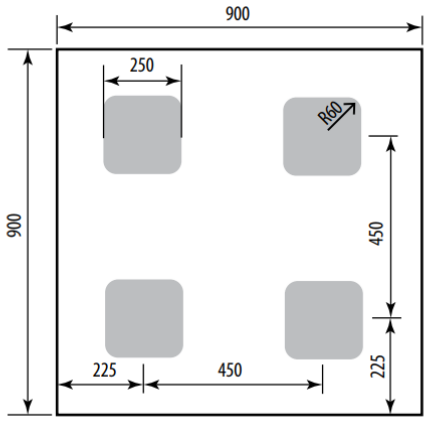
Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Revised January, 2019